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Design Review II

11/12/13

**SUMMARIES**

A 175 mV Multi-Accumulate Unit Using an Adaptive Supply Voltage and Body Bias Architecture [1]

**Synopsys:** This paper discusses a method for reducing power by varying both the supply voltage on a chip and the threshold voltages of the transistors. The authors propose an optimization curve, which can maximally reduce total power (active and leakage) on a chip. The supply and threshold voltages were manually variable; the threshold voltage was controlled by a body bias voltage applied to both nMOS and pMOS transistors.

**Take-Aways:** This paper points out that leakage power becomes a larger part of the total power of a chip as the supply voltage is decreased. It is important to evaluate how changes in supply and threshold voltages affect the performance of a circuit, and to ensure that minimum performance specs are being met as these voltages are scaled.

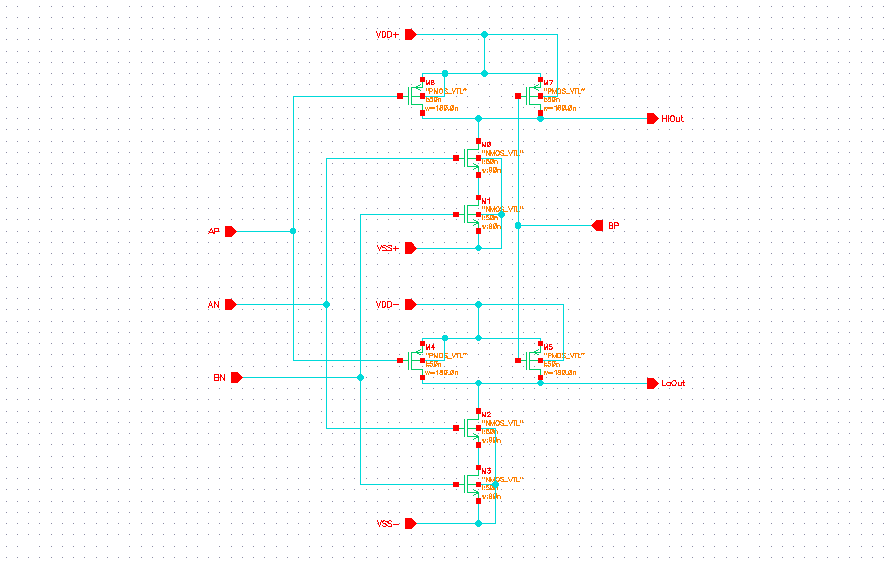
Comparison of Adaptive Body Bias (ABB) and Adaptive Supply Voltage (ASV) for Improving Delay and Leakage Under the Presence of Process Variation [2]

**Synopsys:** This paper addresses the issue of increased impacts of variation with integrated circuit (IC) scaling. The authors discuss the effectiveness of adaptive supply voltage (ASV) as compared to adaptive body bias (ABB) techniques in scaling high performance, low power chips. This comparison was conducted with 0.1-μm CMOS technology and, in particular, examined the impact of ASV and ABB on leakage and delay in an IC. The authors conclude that both ASV and ABB significantly improve leakage and delay. In general, for the 0.1-μm CMOS technology only one or the other (ASV or ABB) is necessary to see peak improvement, though it does depend very slightly on desired yield. Moreover, the authors note that the decision to use ASV as opposed to ABB should be based on a variety of factors, including design complexity, requirements for voltage generation and regulation, reliability, and requirements of silicon overhead [2]. ABB is more expensive due to the requirement of additional silicon area for the bias distribution network. A concern the authors express regarding ASV is reliability. They further note that future CMOS technology may require using both ABB and ASV.

**Take-Aways:** Data from this paper may be useful for comparison to see how the effectiveness of ASV scales, since current CMOS technology is much smaller than the 0.1-μm used in 2003. The authors also suggest future areas of research with respect to ASV, which may be useful for us to consider. Perhaps we can further explore potential side effects of ASV as opposed to ABB.

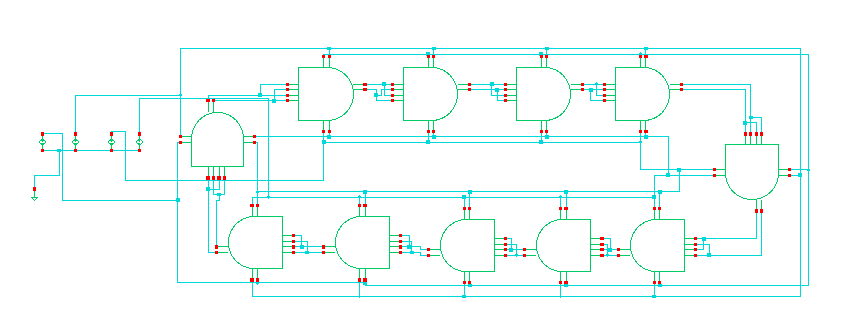
**SIMULATIONS**

Since the first design review and the project proposal, we have expanded our research to applications other than just an inverter. Specifically, we have evaluated the effectiveness of our supply biasing on NAND and NOR gates, and compared the results to NAND and NOR gates which have been body biased. Figure 1 shows the schematic for a NAND gate in a similar configuration to that of the two-inverter gates which were discussed in our previous reviews.



**Figure 1: NAND Gate in Supply Bias Configuration**

As with the two-inverter gates, the supply-biased NAND gate has two outputs; one high output and one low. To test the effectiveness of the supply biasing, we set up 11 of these NAND gates to form a ring oscillator, where the high output of one NAND gate is connected to the NMOS gates of the next NAND gate, and the low output connected to the PMOS gates. Figure 2 shows this configuration.



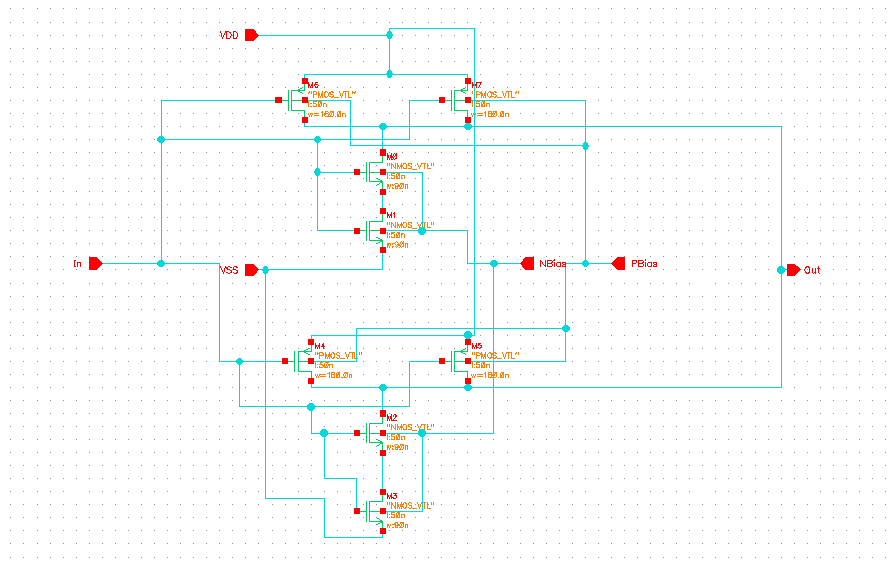
**Figure 2: NAND Gate Test Bench**

This ring oscillator is not particularly useful as an application, but it does allow us to evaluate the response of NAND gates to supply biasing. Figure 3 shows the Power vs. Frequency of this ring oscillator for bias values from -0.1 to 0.05 V. These bias values correspond to how much the top and bottom portion of the NAND gate have been shifted up and down, respectively. For example, a bias value of 0.05 V corresponds to a supply range of 0.05 to VDD + 0.05 for the up-shifted portion, and -0.05 to VDD – 0.05 V for the down-shifted portion of the NAND gate. For this simulation, we used a VDD of 1.1 V.

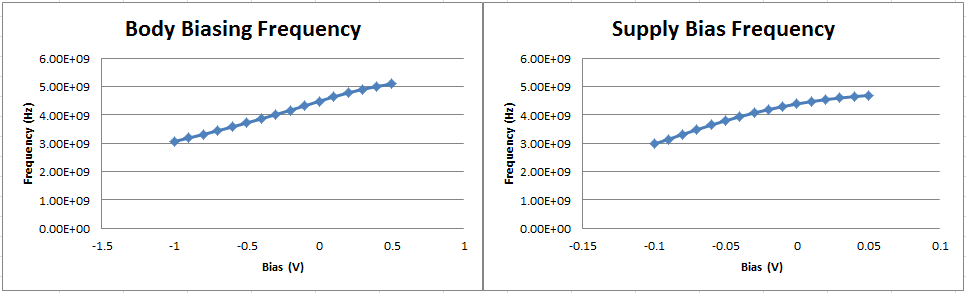
**Figure 3: Power vs. Frequency for NAND Gate Ring Oscillator**

For a ring oscillator with no leakage or short circuit power, we expect this power vs. frequency curve to be linear. However, because leakage current increases exponentially as the bias voltage increases, we see an exponential growth in power.

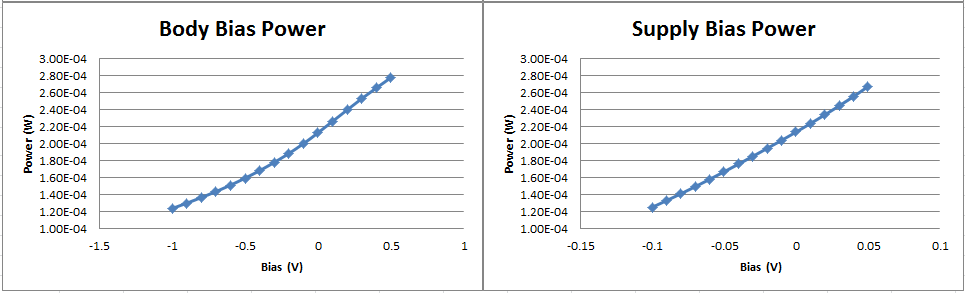
As mentioned before, we compared the results of the supply-biased NAND gate ring oscillator with that of a similar body-biased NAND gate. Figure 4 shows the schematic of this NAND gate. The ring oscillator was setup similarly, and the results for both the body-biased and supply-biased frequency and power are shown in Figure 5.



**Figure 4: Schematic of Body-Biased NAND Gate**



1. (b)

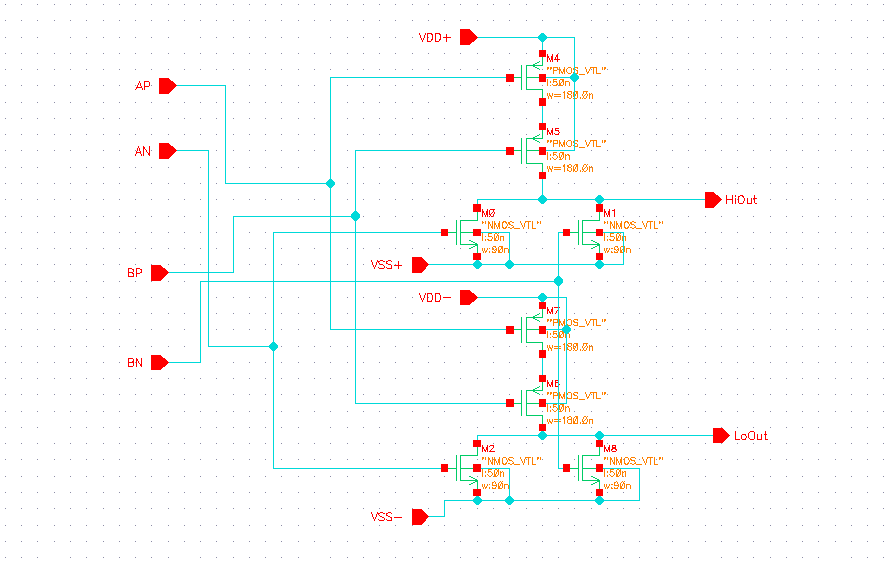


(c) (d)

**Figure 5: Body Bias vs. Supply Bias Frequency (a & b) and Power (c & d) in NAND Ring Oscillator Configuration**

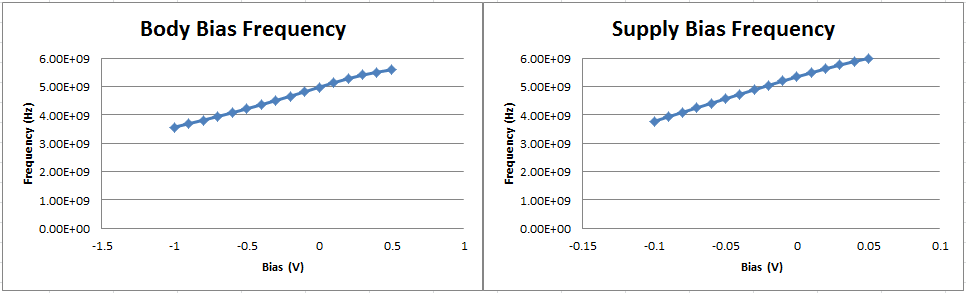
As with the two-inverter gate ring oscillator, the frequency and power for the supply-biased gates were similar to that of the body-biased gates. The supply-biased gates reacted similarly to body-biased gates which were biased with 10 times the voltage as that of the supply-biased gates, just as the two-inverter gates responded.

Similar to the NAND Gate methodology, we also sought to confirm that a supply-biased NOR gate in a ring oscillator configuration would give us results similar to body biasing. Figure 6 shows the schematic for the supply-biased NOR gate.

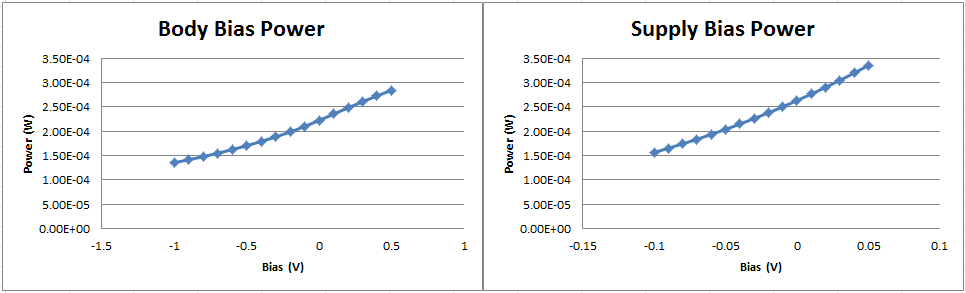


**Figure 6: Schematic of Supply-Biased NOR Gate**

The body-biased NOR gate was constructed similarly to the body-biased NAND gate. Figure 7 shows the power and frequency of the supply and body-biased NOR ring oscillator.



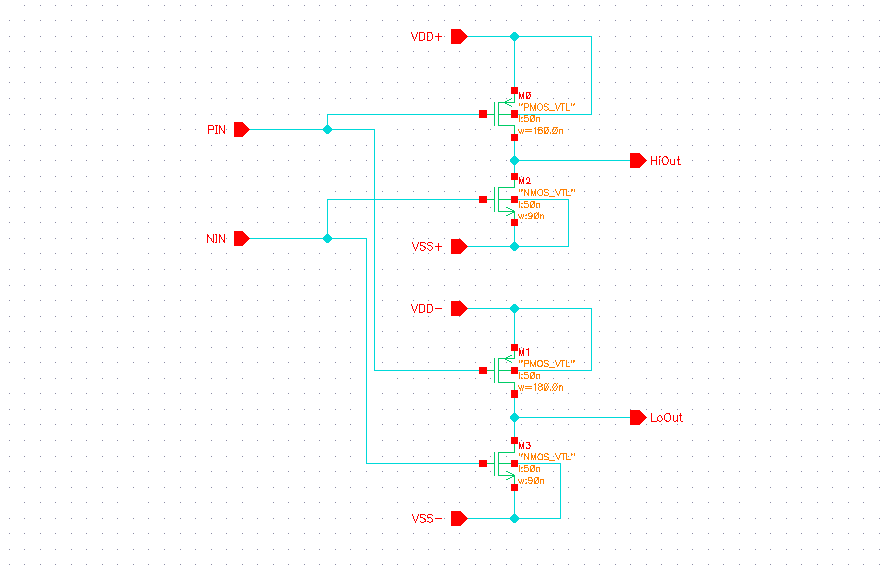
1. (b)



(c) (d)

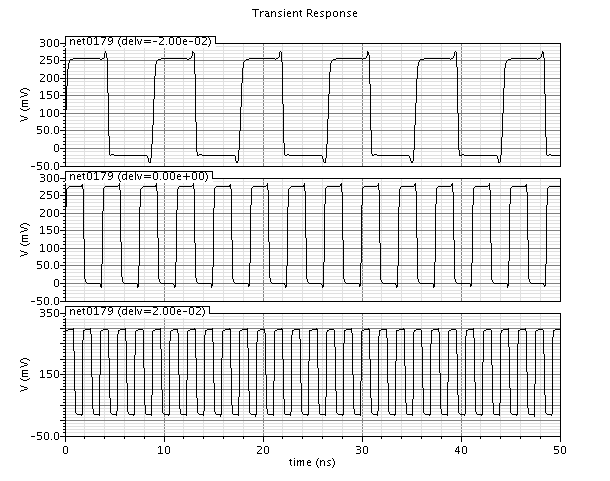
**Figure 7: Body Bias vs. Supply Bias Frequency (a & b) and Power (c & d) in NOR Ring Oscillator Configuration**

All of these simulations have been conducted with a VDD of 1.1 V, but we want to confirm that these techniques work for in sub-threshold conditions as well. Therefore, we conducted a short analysis of the inverter gates with the supply voltage less than the threshold voltage. Figure 8 reminds the reader of the two-inverter gate that was first tested before design review I.



**Figure 8: Supply-Biased Two-Inverter Gate**

We used a nominal voltage of 0.275 V (Vt is about 0.4 V for this technology). Figure 9 shows the waveform for bias voltages of -0.02 V, 0 V, and 0.02 V.



**Figure 9: Two-Inverter Gate Ring Oscillator Sub-Threshold Response**

There is a sharp increase in frequency as the bias voltage increases. Because sub-threshold operation deals only with leakage voltage, the frequency is expected to change exponentially because leakage current increases exponentially with Vgs.

**REPORT**

**Current Progress**

Since the proposal, we have moved on to simulating ring oscillators constructed from supply voltage biased 4-input, 2-output NAND and NOR gates. They present very similar results to the inverter-constructed ring oscillator (see simulations), demonstrating the effectiveness of supply voltage biasing on these other commonly used gates. We opted to pursue the above applications instead of exploring leakage and short circuit currents as depicted in our project proposal.

**Challenges and New Design Considerations**

Thus far, we have designed our gates such that there is one half of the gate shifted up by some bias voltage, and one half shifted down by the same voltage, but the difference in supply voltages for each half of the gate is still VDD. We have scheduled a tape out for February which will incorporate some application of these gates, and we therefore need to begin realizing a way to obtain these voltage differences and ranges. We have begun brainstorming ideas to be tested in the next few weeks. One such idea is to only shift one half up by twice the bias while keeping the bottom half supplies at 0 and VDD. This will require that only two voltages other than that supplied to the chip will need to be maintained (VSS+ and VDD+). This is expected to yield similar results related to frequency and power consumption. Another idea is to supply the up-shifted gate with voltages ranging from 0 + the bias voltage to VDD, and the downshifted gate with voltages ranging from 0 to VDD – the bias voltage. The advantage here is that this design will not require a charge pump, but problems may arise due to the difference in the supply voltages to each “half” gate changing as the bias voltage changes. As stated before, these ideas will be either confirmed or proven faulty in the upcoming weeks.

**Next Steps**

The successful results from simulated applications thus far have given us motivation to move on to testing applications beyond the ring oscillator. These applications include a half adder, a full adder, and a multiplier. At the gate level, we will apply the same supply-biasing techniques tested in the ring oscillators and see if we can create a “knob” for changing the delay and/or power of these applications.

**References**

[1] Kao, James T., Masayuki Miyazaki, and A. R. Chandrakasan. "A 175-mV multiply-accumulate unit using an adaptive supply voltage and body bias architecture." *Solid-State Circuits, IEEE Journal of* 37.11 (2002): 1545-1554. 11 Nov 2013.

[2] Chen, Tom, and Samuel Naffziger. "Comparison of adaptive body bias (ABB) and adaptive supply voltage (ASV) for improving delay and leakage under the presence of process variation." *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 11.5 (2003): 888-899. 11 Nov 2013.